

2. If n-transistor conducts and has large voltage between source and drain, then it is said to be in \_\_\_\_\_ region  
a) linear  
b) saturation  
c) non saturation  
d) cut-off

Answer: b  
Explanation: If n-transistor conducts and has large voltage between source and drain, then it is in saturation.

3. If p-transistor is conducting and has small voltage between source and drain, then the it is said to work in  
a) linear region  
b) saturation region  
c) non saturation resistive region  
d) cut-off region

Answer: c  
Explanation: If p-transistor is conducting and has small voltage between source and drain, then it is said to be in unsaturated resistive region.

4. In the region where inverter exhibits gain, the two transistors are in \_\_\_\_\_\_\_ region  
a) linear  
b) cut-off  
c) non saturation  
d) saturation

Answer: d  
Explanation: In the region where the inverter exhibits gain, the two transistors n and p operates in saturation region.

5. If both the transistors are in saturation, then they act as  
a) current source  
b) voltage source  
c) divider  
d) buffer

Answer: a  
Explanation: When both the transistors are in saturation, then act as current sources so that the equivalent circuit is two current sources between Vdd and Vss.

If βn = βp, then Vin is equal to  
a) Vdd  
b) Vss  
c) 2Vdd  
d) 0.5Vdd

Answer: d  
Explanation: If βn = βp, then Vin = 0.5Vdd which implies that the changeover between logic levels is symmetrically disposed about the point

Mobility depends on  
a) transverse electric field  
b) Vg  
c) Vdd  
d) Channel length

Answer: a  
Explanation: Mobility is affected by transverse electric field and thus also depends on Vgs and the mobility of p-device and n-device are inherently unequal

8. In CMOS inverter, transistor is a switch having  
a) infinite on resistance  
b) finite on resistance  
c) buffer  
d) infinite off resistance

Explanation: In CMOS inverter, transistor is a awitch having finite on resistance and infinite off resistance.

9. CMOS inverter has \_\_\_\_\_\_ output impedance  
a) low  
b) high

Answer: a  
Explanation: CMOS inverter has low output impedance and this makes it less prone to noise and disturbance.

10. Input resistance of CMOS inverter is  
a) high  
b) low

Answer: a  
Explanation: Input resistance of CMOS inverter is extremely high as it is a perfect insulator and draws no dc input source.

11. Increasing fan-out, \_\_\_\_\_\_ the propogation delay  
a) increases  
b) decreases  
c) does not affect  
d) exponentially decreases

Answer: a  
Explanation: In CMOS inverter, increasing the fan-out also increases the propogation delay. Fan-out is a term that defines the maximum number of digital inputs that the output of a single logic gate can feed.

12. Fast gate can be built by keeping  
a) low output capacitance  
b) high on resistance  
c) high output capacitance  
d) input capacitance does not affect speed of the gate

Answer: a  
Explanation: Fast gate can be built by keeping the output capacitance small and by decreasing the on resistance of the transistor.

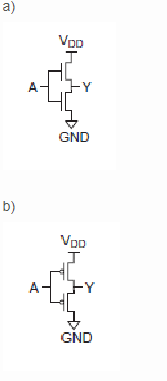
13. In negative logic convention, the Boolean Logic [1] is equivalent to:  
a) +VDD  
b) 0 V  
c) -VDD  
d) None of the mentioned

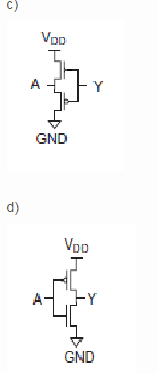
Answer : b  
Explanation: In negative logic convention, the Boolean Logic [1] is equivalent to 0 V and Logic ‘0’ is equivalent to +VDD

14. In positive logic convention, the true state is represented as:  
a) 1  
b) 0  
c) -1  
d) -0

Answer: a  
Explanation: In positive logic convention, the Boolean logic ‘1’ is known to be representing true state.

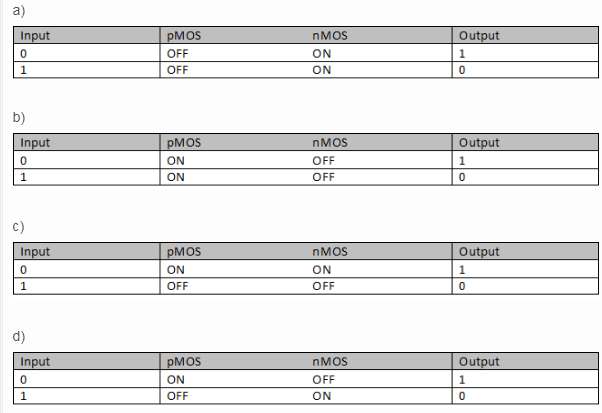
15.The CMOS gate circuit of NOT gate is:





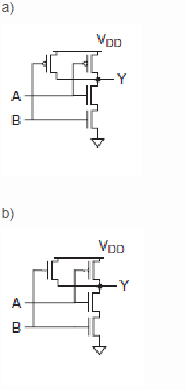
Answer: d  
Explanation: The CMOS logic circuit for NOT gate has a p-MOS as a pull up transistor and n-MOS as driver transistor which is represented accurately in figure (d)

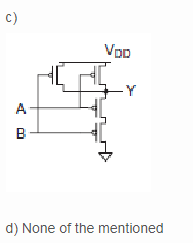
16. The truth table which accurately explains the operation of CMOS not gate is:



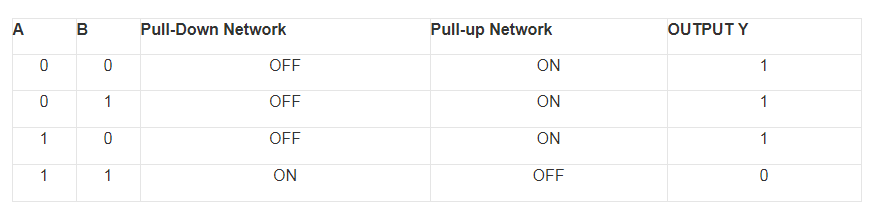
Answer: d  
Explanation: The output of CMOS depends on the state of nMOS and pMOS transistor

17. The CMOS logic circuit for NAND gate is:





Answer: a



18. In CMOS logic circuit the n-MOS transistor acts as:

a) Load  
b) Pull up network  
c) Pull down network  
d) Not used in CMOS circuits

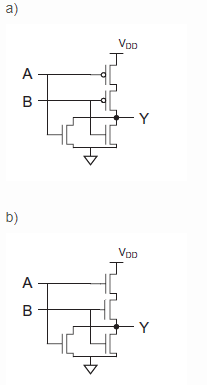
Answer: c  
Explanation: A static CMOS gate has an nMOS pull-down network to  
connect the output to 0 (GND)

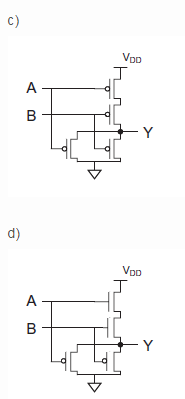
19. In CMOS logic circuit the p-MOS transistor acts as:  
a) Pull down network  
b) Pull up network  
c) Load  
d) Short to ground

Answer: b  
Explanation: A static CMOS gate has an pMOS pull-up network to  
connect the output to VDD (1)

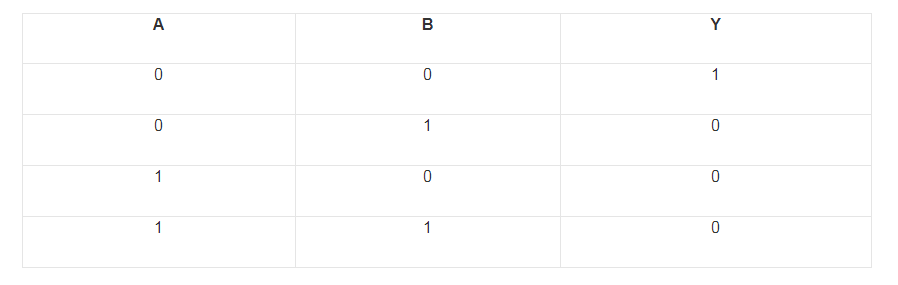
20. In CMOS logic circuit, the switching operation occurs because:  
a) Both n-MOSFET and p-MOSFET turns OFF simultaneously for input ‘0’ and turns ON simultaneously for input ‘1’  
b) Both n-MOSFET and p-MOSFET turns ON simultaneously for input ‘0’ and turns OFF simultaneously for input ‘1’  
c) N-MOSFET transistor turns ON, and p-MOSFET transistor turns OFF for input ‘1’ and N-MOS transistor turns OFF, and p-MOS transistor turns ON for input ‘0’  
d) None of the mentioned

Answer: c  
Explanation: In CMOS logic circuit, the switching operation occurs because N-MOS transistor turns ON, and p-MOS transistor turns OFF for input ‘1’ and N-MOS transistor turns OFF, and p-MOS transistor turns ON for input ‘0’. The networks are arranged such that one is ON and the other OFF for any input pattern.  
21. The CMOS logic circuit for NOR gate is





Answer: a



22. When both nMOS and pMOS transistors of CMOS logic design are in OFF condition, the output is :  
a) 1 or Vdd or HIGH state  
b) 0 or ground or LOW state  
c) High impedance or floating(Z)  
d) None of the mentioned

Answer: c

23. When both nMOS and pMOS transistors of CMOS logic gates are ON, the output is :  
a) 1 or Vdd or HIGH state  
b) 0 or ground or LOW state  
c) Crowbarred or Contention(X)  
d) None of the mentioned

Answer: c  
Explanation: The crowbarred (or contention) X level exists when both pull up and pull down transistors are simultaneously turned ON. Contention between the two networks results in an indeterminate output level and dissipates static power.